AF 2134

TRANSMITTAL FORM

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Application No.	09/672,367
Filing Date	September 28, 2000
First Named Inventor	Francis X. McKeen
Art Unit	2134
Examiner Name	Thomas M. Ho
Total Number of Pages in This Submission	32
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ENCLOSURES ***(check all that apply)***

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Response
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  - [ ] Affidavits/declaration(s)
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- [ ] Information Disclosure Statement
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- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Thomas M. Coester, Reg. No. 39,637 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Thomas Coester
Date	February 10, 2006

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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
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☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

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FEE CALCULATION

1. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	22	- 22** =	0	x	50.00	=	$0.00
Independent Claims	3	- 3** =	0	x	200.00	=	$0.00
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple Dependent claim, if not paid
1204	790	2204	395	**Reissue independent claims over original patent
1205	300	2205	150	**Reissue claims in excess of 20 and over original patent

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2. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify)					
				SUBTOTAL (2)	($) 500.00

SUBMITTED BY Complete (if applicable)

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Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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Attorney's Docket No. 42P9578

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Examiner:	**Ho, Thomas M.**
Francis X. McKeen	)	Art Group:	**2134**
Serial No. 09/672,367	)		
Filed: September 28, 2000	)		
For: **A MECHANISM TO SECURE COMPUTER OUTPUT FROM SOFTWARE ATTACK USING ISOLATED EXECUTION**	)		

Assistant Commissioner for Patents
Board of Patent Appeals and Interferences
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Pursuant to 37 C.F.R. § 41.37, Applicant submits the following Appeal Brief for consideration by the Board of Patent Appeals and Interferences ("Board"). Applicant also submits herewith a check in the amount of $500.00 to cover the cost of filing this opening brief, as set forth in 37 C.F.R. § 41.20(b)(2). Please charge any additional amounts due or credit any overpayment to Deposit Account No. 02-2666.

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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Francis X. McKeen, et al, the parties named in the caption, transferred their rights in that which is disclosed in the subject application through an assignment recorded on January 2, 2001 to Intel Corporation. Accordingly, Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-22 are pending in this application. All claims stand rejected. Applicant seeks review of claims 1-22.

IV. STATUS OF AMENDMENTS

No amendments have been requested, and none have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed subject matter relates to securing output data in an isolated execution environment (Field of Invention). Embodiments include a method and a platform for maintaining the security of output data in an isolated execution environment (Abstract).

The disclosed architecture includes an isolated area in the system memory, which is protected by components of the platform (e.g., the processor and chipset) (P.5, lines 28-30). Access to the isolated area is restricted to the processor executing in an isolated execution mode (P.6, lines 2-4). An isolated output area is partitioned within the main memory (P.6, lines 5-6). The isolated output area is only readable by an

output device in an isolated execution mode and writable by an O/S nub via an output driver (P.6, lines 6-8).

The disclosed architecture also includes a memory control hub (MCH) coupled between the system memory and the processor (P.12, lines 17-18). The MCH is also coupled to an output device, such as a graphics card, by a secure AGP bus (P.13, lines 3-4).

Three independent claims, 1, 12, and 19, and nineteen dependent claims (2-11, 13-18 and 20-22) are presented in this appeal.

Independent claim 1 recites a platform comprising a processor executing in one of a normal execution mode and an isolated execution mode (P.5, lines 11-12 and lines 23-25; FIG. 1A, features 11, 21, 31, 41, 15, 25, 35, and 45); a system memory including an isolated area, an isolated output area, and a non-isolated area (P.7, lines 6-10; P.6, lines 5-6; FIG.1B, features 60, 70, 80, and 90; FIG.2, features 270, 280, and 290); and an output device (P.8, line 9; FIG.1C, feature 175).

Dependent claim 2 modifies the platform of claim 1 to recite that the output device is a graphics card (P.13, line 3; FIG.2, feature 275).

Dependent claim 3 modifies the platform of claim 2 to include a memory control hub (MCH) coupled between the system memory, and the processor and the graphics card (P.9, lines 18-20; FIG.1C, feature 130; FIG.2, feature 230), the memory control hub to permit the graphics card to access the isolated output area only when the graphics card is in isolated access mode (P.13, lines 6-8).

Dependent claim 4 modifies the platform of claim 3 to include a direct memory access (DMA) controller and wherein local storage of the data from the isolated output area is not permitted (P.13, lines 10-13).

Dependent claim 5 modifies the platform of claim 3 to recite that only the graphics card is permitted to read the isolated output area (P.13, lines 3-9).

Dependent claim 6 modifies the platform of claim 1 to include an operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in isolated execution mode (P.12, lines 22-29; FIG.2, features 216 and 217).

Dependent claim 7 modifies the platform of claim 3 to include a link between the graphics card and the MCH having an isolated transaction type (P.13, lines 3-4).

Dependent claim 8 modifies the platform of claim 3 to recite that the MCH only permits the O/S nub to write to the isolated output area (P.12, line 22 – P.13, line 2).

Dependent claim 9 modifies the platform of claim 7 to recite that the link is a secure accelerated graphics port bus (P.13, lines 3-4; FIG.2, feature 252).

Dependent claim 10 modifies the platform of claim 10 to recite that the graphics card comprises an isolated bit plane; and a non-isolated bit plane (P.13, lines 13-14).

Dependent claim 11 modifies the platform of claim 10 to recite that the graphics card denies all external access to the isolated bit plane (P.13, lines 18-19).

Independent claim 12 is drawn to a method comprising establishing an isolated execution environment having an isolated execution mode (P.5, lines 8-9; FIG.1A, feature 50); and preventing access to output data by any requester not operating in an isolated mode (P.6, lines 15-16).

Dependent claim 13 modifies the method of claim 12 to recite segregating a system memory into an isolated output area and a non-isolated area (P.7, lines 6-10; FIG.1B, feature 60).

Dependent claim 14 modifies the method of claim 13 to recite issuing an isolated direct memory access (DMA) request for display data in the isolated output area from a graphics card (P.13, lines 6-8 and 21-22); and refreshing the display based on the display data (P.13, lines 22-23).

Dependent claim 15 modifies the method of claim 13 to recite identifying if an isolated attribute is present in a request for access to the isolated output area (P.12, lines 24-26); and denying the request if no isolated attribute is present (P.12, lines 26-28).

Dependent claim 16 modifies the method of claim 13 to recite loading data from the isolated output area into a bit plane on a graphics card (P.13, lines 13-14); and denying all external access to the bit plane (P.13, lines 18-19).

Dependent claim 17 modifies the method of claim 16 to recite defining a first window for display of an image corresponding to the bit plane (P.13, lines 29-30); and occluding all windows but the first window (P.14, lines 1-2).

Dependent claim 18 modifies the method of claim 13 to recite retrieving data from the isolated output area (P.13, lines 6-8); displaying an image corresponding to the data (P.13, lines 29-30); and occluding the image prior to a platform transitioning out of isolated execution mode (P.14, lines 1-2).

Independent claim 19 is drawn to a platform comprising a processor executing in one of a normal execution mode and an isolated execution mode (P.5, lines 8-9; FIG.1A, feature 50); a direct memory access (DMA) controller to issue requests for access to an isolated output area (P.13, lines 10-13); a first interface coupled to the DMA controller to forward requests to a memory control hub (MCH) (P.13, lines 6-8); and a second interface coupled to the DMA controller to supply output data to an output device (P.14, lines 9-11).

Dependent claim 20 modifies the platform of claim 19 to recite the first interface is a secure accelerated graphics port (AGP) and the output device is a display (P.13, lines 6-8 and 12).

Dependent claim 21 modifies the platform of claim 19 to recite the DMA controller attaches an isolated attribute to any isolated output area access request (P.13, lines 6-25).

Dependent claim 22 modifies the platform of claim 19 to recite the second interface is an audio interface (P.14, lines 9-11).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-22 stand rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,935,247 issued to Pai *et al.* ("Pai") in view of the article "AGP Video System Memory Access" published by the PC Guide ("PC").

VII. ARGUMENT

A. Overview of Cited References

1. U.S. Patent No. 5,935,247 issued to Pai *et al.* ("Pai").

Pai discloses a computer system having a genetic code that cannot be directly accessed by processors or other master devices (Abstract). The computer system includes a processor 2, a genetic code memory 4, a display mode controller 10, a data switch device 20, a converter 30, a display buffer 40, and a monitor 42 (col.3, lines 13-22; FIG. 1, features 2, 4, 10, 20, 30, 40, and 42). During a Genetic Code Display Procedure (GDP), two text strings respectively from processor 2 and converter 30 are merged and stored in display buffer 40 (Col. 3, lines 59-62). The text string from processor 2 is sent to an input terminal A of data switch device 20. The other text string from converter 30 is sent to an input terminal B of data switch device 20. The merge operation is controlled by display mode controller 10, which generates an EN signal to electrically connect either input terminal A or B to an output terminal (col.4, lines 5-7). The output terminal is connected to display buffer 40. Data stored in display buffer 40 cannot be read from the input terminals of data switch device 20 (col.5, lines 47-48). Driven by a video display card (not shown) and according to the temporarily merged string, monitor 42 may show the true genetic code on the screen (col.3, lines 62-64).

Pai does not teach or suggest a system memory including an isolated output area. Pai at most mentions display buffer 40 and peripheral memory which are not part of a system memory.

2. The article "AGP Video System Memory Access" published by the PC Guide ("PC").

PC discloses an AGP video system having the ability to share a main system memory with a video chipset (paragraph 1). However, under the AGP, not all of the video card's memory is taken from the main system memory (paragraph 2). Under the AGP, the frame buffer remains on the video card, where it belongs (paragraph 2). The

frame buffer is the most important part of the video memory and it requires the highest performance, so it makes sense to leave it on the video card (paragraph 2). Thus, special video-specific technologies like VRAM can be used for the frame buffer (paragraph 2).

PC is relied upon for its alleged disclosure of performing video function on the system memory. However, PC specifically teaches that the frame buffer should remain on the video card. Thus, PC does not cure the deficiency of Pai for failing to disclose the system memory including an isolated output area.

B. Claims Rejected Under 35 U.S.C. § 103(a)

Claims 1-22 stand under 35 U.S.C. § 103(a) as obvious over Pai in view of PC. For the reasons discussed below, Applicant disagrees that the cited references disclose all the limitations of the rejected claims.

1. Regarding Claim 1

Applicant notes that Pai at least fails to disclose a system memory including an isolated output area. It is disclosed in Applicant's specification (P.6, lines 5-6; FIG. 1B, feature 60 and FIG. 1C, feature 140) that the term "system memory," consistent with the common usage of the term in the art, means the main memory which is physically separated from the memory located on a peripheral device. According to the definition, system memory is used synonymously with main memory. Thus, if an output memory (e.g., a frame buffer, a display buffer, or a video card memory) is physically located on an output device (e.g., a monitor or a video card), that output memory does not belong to and is not part of the system/main memory.

The term "isolated output area" is characterized by the Examiner as a video (card) memory (P.3, lines 1-2 of Final Office Action). If the video card memory is defined as the memory physically located on the video card, the video card memory by definition cannot be the system/main memory. Thus, the memory located on the video card cannot be the claimed isolated output area in the system/main memory.

If the video card memory refers to the frame buffer, e.g. display buffer 40 of Pai, the frame buffer also cannot be the isolated output area in the system/main memory. The Examiner relies on PC for disclosing the sharing of the system memory space by a video card. Even assuming, solely for the sake of argument, that the video card uses part of the system/main memory which is physically located outside of the video card for video functions, the frame buffer or the display buffer of the video card should remain on the video card. This is because PC specifically teaches that using the main system memory for the frame buffer would be an ill-fated approach. Thus, PC has taught away using the system/main memory as the frame buffer or display buffer 40. That is, display buffer 40 should physically remain on the video card. Thus, according to the teaching of PC, display buffer 40 is not part of the system/main memory and thus cannot be the isolated output area in the system/main memory.

The Examiner characterizes the memory space at the output end of switch 20 as the isolated output area, and asserts that a portion of this memory space may be the system memory. However, Pai at most mentions display buffer 40, monitor 42, and a video display card at the output end of switch 20. Thus, according to Pai, the memory space for the alleged isolated output area physically resides in display buffer 40, monitor 42, or the video display card. Display buffer 40 resides on a video card according to the teaching of PC. The video card, monitor 42, and the video display card are peripheral devices and thus cannot possibly house the system/main memory.

In Pai, the output area isolated from the processor is physically located at the output of switch 20. Without the protection of switch 20, the output to display buffer 40 would not be isolated. Thus, for this "isolated output area" to remain isolated, the teaching of Pai requires the isolated output area be located at the output of switch 20. In the attempt to characterize a portion of the system memory as isolated and shared by the video card, the Examiner seems to indicate a portion of the system memory resides at the output end of switch 20. This characterization contradicts the plain teaching of Pai where only peripheral memory resides at the output end of switch 20. A skilled person would understand memory closely associated with peripheral devices as peripheral memory. A peripheral memory is not the system/main memory.

For at least these reasons, Applicant respectfully submits that Pai in view of PC does not teach or suggest a system memory including an isolated output area. Thus, the Board should overturn the rejection of claim 1.

2. Regarding Claim 2

Claim 2 depends from claim 1 and incorporates the limitations thereof. Thus, for at least the reasons mentioned above in regard to claim 1, Pai in view of PC does not teach or suggest each of the elements of claim 2.

Moreover, claim 2 further recites that the output device is a graphics card. The cited paragraphs (col.3, line 62 to col.4, line 1) at most mention a video display card that is used to drive display buffer 40. The video display card is responsible for driving a text string onto a video display device, such as a monitor. Pai does not mention any graphics to be displayed. The display of a text string does not require a graphics card. There is nothing in Pai that suggests a graphics card. PC also does not supply a reason why a graphics card should be used in the system of Pai. Thus, for at least these reasons, Applicant respectfully submits that claim 2 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 2.

3. Regarding Claim 3

Claim 3 depends from claim 2 and incorporates the limitations thereof. Thus, for at least the reasons mentioned above in regard to claim 2, Pai in view of PC does not teach or suggest each of the elements of claim 3.

Moreover, claim 3 further recites a memory control hub (MCH) coupled between the system memory, the processor, and the graphics card. The Examiner relies on FIG. 3 of Pai for teaching the claimed MCH. Specifically, the Examiner points to Input Mode Synchronization Register 50 and switch 90 as the claimed MCH. However, elements 50 and 90, as shown in FIG. 3, are located between the processor, the input device, and the genetic code memory (which is characterized by the Examiner as part of the system memory). These elements are not connected, directly or indirectly, to a graphics card or any output device. Thus, elements 50 and 90 cannot possibly be the claimed MCH. For

the same reason, elements 50 and 90 cannot possibly "permit the graphics card to access the isolated output area only when the graphics card in isolated access mode" as recited in claim 3.

Thus, for at least these reasons, Applicant respectfully submits that claim 3 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 3.

4. Regarding Claim 4

Claim 4 depends from claim 3 and incorporates the limitations thereof. Thus, for at least the reasons mentioned above in regard to claim 3, Pai in view of PC does not teach or suggest each of the elements of claim 4.

Moreover, claim 4 further recites "a direct memory access (DMA) controller and wherein local storage of the data from the isolated output area is not permitted." The cited paragraphs of Pai (col.4, lines 44-48 and col.5, lines 45-50) are silent on using a DMA controller for data transfer. The Examiner asserts that "the DMA controller is understood to be there in order to be able to access the memory (display buffer) and its video card memory." However, accessing a display buffer or a video card memory does not generally require a DMA controller. Further, the cited paragraphs at most teach preventing processor 2 from accessing display buffer 40. There is nothing in the cited paragraphs mentioning that "local storage of the data from the isolated output area is not permitted," as required by claim 4.

Thus, for at least these reasons, Applicant respectfully submits that claim 4 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 4.

5. Regarding Claim 5

Claim 5 depends from claim 3 and incorporates the limitations thereof. Thus, for least the reasons mentioned above in regard to claim 3, Pai in view of PC does not teach or suggest each of the elements of claim 5.

Moreover, claim 5 further recites that "only the graphics card is permitted to read the isolated output area." Even for the sake of argument that the video display card mentioned in Pai were to be characterized as a graphics card, there is no teaching or suggestion that "only the graphics card is permitted to read the isolated output area" as claimed. Pai at most discloses preventing processor 2 from accessing display buffer 40. After the data reaches display buffer 40, it is unclear whether other devices connected to display buffer 40, if any, have access to the display buffer. Pai does not teach or suggest which devices are permitted to read display buffer 40 and whether the video display card is the only device that is permitted to read from the buffer.

Thus, for at least these reasons, Applicant respectfully submits that claim 5 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 5.

6. Regarding Claim 6

Claim 6 depends from claim 1 and incorporates the limitations thereof. Thus, for at least the reasons mentioned above in regard to claim 1, Pai in view of PC does not teach or suggest each of the elements of claim 6.

Moreover, claim 6 further recites "an operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in isolated execution mode." The concept of using an O/S nub is totally absent in Pai. The O/S nub is not explicitly disclosed by Pai nor inherently required by the system of Pai. The cited paragraphs of Pai (col.4, lines 49-57) are completely silent on using a driver of an O/S nub to write to the isolated output area. As recognized by the Examiner in the rejection of claims 2 and 5, it is the video display card that drives the data from display buffer 40 to the monitor. This point is confirmed by the disclosure of Pai at col. 3, line 62, which is cited by the Examiner in the rejection of claim 2. There is nothing in Pai or elsewhere in the cited art that teaches or suggests the O/S nub having a driver to write the data as claimed.

Thus, for at least these reasons, Applicant respectfully submits that claim 6 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 6.

7. Regarding Claim 7

Claim 7 depends from claim 3 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 3, Pai in view of PC does not teach or suggest each of the elements of claim 7.

Moreover, claim 7 further recites "a link between the graphics card and the MCH having an isolated transaction type." For at least the reasons mentioned above in regard to claims 2 and 3, neither reference teaches or suggests the claimed graphics card or the MCH. Thus, the cited references cannot possibly disclose or suggest the link between the graphics card and the MCH. Even for the pure sake of argument that the video display card is the claimed graphics card and elements 50 and 90 are the claimed MCH (FIG. 3 of Pai), there is no link or any connection existing between the video display card and elements 50 and 90. Thus, the cited references cannot possibly teach or suggest the link between the graphics card and the MCH as claimed.

Thus, for at least these reasons, Applicant respectfully submits that claim 7 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 7.

8. Regarding Claim 8

Claim 8 depends from claim 3 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 3, Pai in view of PC does not teach or suggest each of the elements of claim 8.

Moreover, claim 8 further recites that "the MCH only permits the O/S nub to write to the isolated output area." The cited references not only fail to mention the MCH or the O/S nub, but also fail to disclose that "the MCH only permits the O/S nub" to write to the isolated output area. Assuming for the sake of argument that display buffer 40 is the isolated output area, both processor 2 and converter 30 are

allowed to write to display buffer 40 as each of them writes half of the output text string. Thus, according to Pai, at least two separate devices are allowed to write to the isolated output area. Thus, the O/S nub cannot be said to be the the only permitted write to what the Examiner characterizes as the isolated output area.

Thus, for at least these reasons, Applicant respectfully submits that claim 8 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 8.

9. Regarding Claim 9

Claim 9 depends from claim 7 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 3, Pai in view of PC does not teach or suggest each of the elements of claim 9.

Moreover, claim 9 further recites that "the link is a secure accelerated graphics port bus." The cited references not only fail to mention the link between the graphics card and the MCH, but also fail to disclose that the link is a secure accelerated graphics port (AGP) bus. The Examiner asserts that Pai teaches the AGP bus because all video cards are graphics acceleration devices. However, as is generally known in the art, the AGP bus is an industry standard that defines a bus interface. AGP bus is one bus standard out of many bus standards. Thus, not "all" video cards use the AGP bus. Further, none of the cited references mention or suggest any graphics port bus that is "secure." The cited references do not mention any graphics port bus, let alone a secure graphics port bus.

Thus, for at least these reasons, Applicant respectfully submits that claim 9 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 9.

10. Regarding Claim 10

Claim 10 depends from claim 2 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 2, Pai in view of PC does not teach or suggest each of the elements of claim 10.

Moreover, claim 10 further recites that "the graphics card comprises an isolated bit plane and a non-isolated bit plane." The concept of "bit plane" is totally lacking in the cited references. The display of a text string, as taught by Pai, does not require the storage of bit planes. Pai does not disclose displaying graphics, and PC does not provide any motivation for displaying graphics in Pai's system. Thus, there is no motivation to modify Pai to include a graphics card in the system or to include the storage of bit planes in the graphics card.

Thus, for at least these reasons, Applicant respectfully submits that claim 10 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 10.

11. Regarding Claim 11

Claim 11 depends from claim 10 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 10, Pai in view of PC does not teach or suggest each of the elements of claim 11.

Moreover, claim 11 further recites that "the graphics card denies all external access to the isolated bit plane." Even for the sake of argument that the video display card is the graphics card, there is nothing in the cited references that mention or suggest "the graphics card denies all external access to the isolated bit plane." The disclosure of Pai at most mentions that the video display card (col.3, line 62) drives the data in display buffer 40 for display on the monitor. There is nothing that teaches or suggests that the video display card takes on the role of permitting or denying external access to the isolated bit plane.

Thus, for at least these reasons, Applicant respectfully submits that claim 11 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 11.

12. Regarding Claim 12

In regard to independent claim 12, Applicant submits that Pai at least fails to disclose the limitation of "preventing access to output data by any requester not operating in an isolated mode," as recited in claim 12.

The Examiner rejects claim 12 for the same reasons that claim 1 is rejected. However, the cited references at most disclose that processor 2 is prevented from reading the data in display buffer 40. Other devices, e.g., the video display card, is not prevented from accessing the data in display buffer. In the Final Office Action at page 4, paragraph 3, the Examiner characterizes the Genetic Code Display Procedure (GDP) as the isolated mode. Even for the sake of argument that the GDP is the isolated mode, the video display card is able to access the data in display buffer 40 for display on the monitor whether or not the system is executing the GDP. Further, according to the Examiner's assertion, processor 2 would be in the isolated mode when the system is executing the GDP. However, this assertion contradicts with Pai's teaching that processor 2 is prevented from accessing the data in display buffer 40 even though processor 2 is executing the GDP.

PC does not cure the defect of Pai. There is nothing in PC that mentions or suggests any isolated mode or preventing access to output data.

Thus, for at least these reasons, Applicant respectfully submits that claim 12 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 12.

13. Regarding Claim 13

Claim 13 depends from claim 12 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 12, Pai in view of PC does not teach or suggest each of the elements of claim 13.

Moreover, claim 13 further recites "segregating a system memory into an isolated output area and a non-isolated area." Pai in view of PC does not teach or suggest an isolated output area as part of the system memory. As mentioned above in regard to

claim 1, the video card memory cannot possibly disclose or suggest that the claimed isolated output area is part of the system memory.

Thus, for at least these reasons, Applicant respectfully submits that claim 13 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 13.

14. Regarding Claim 14

Claim 14 depends from claim 13 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 13, Pai in view of PC does not teach or suggest each of the elements of claim 14.

Moreover, claim 14 further recites "issuing an isolated direct memory access (DMA) request for display data in the isolated output area from a graphics card; and refreshing the display based on the display data." Pai in view of PC does not teach or suggest issuing a DMA request. The cited paragraph at most mentions that the display of the text string uses "conventional video driving technique" (col.5, lines 29-30). A conventional video driving technique does not require issuing a DMA request. In fact, the concept of DMA is totally lacking in the cited references. There is nothing in the cited references that even suggest the DMA request.

Thus, for at least these reasons, Applicant respectfully submits that claim 14 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 14.

15. Regarding Claim 15

Claim 15 depends from claim 13 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 13, Pai in view of PC does not teach or suggest each of the elements of claim 15.

Moreover, claim 15 further recites "identifying if an isolated attribute is present in a request for access to the isolated output area; and denying the request if no isolated attribute is present." The cited references do not teach or suggest identifying an isolated attribute. Specifically, the concept of an "isolated attribute" is totally lacking in

the cited references. The Examiner characterizes the isolated attribute as "any one of the starting mechanisms that initiates the GDP, the value of the synchronization mode logic, or the value of the enable signal of the data switch device" (page 12, first paragraph of Final Office Action). However, this characterization would render processor 2 as having the isolated attribute, because the GDP is a procedure initiated by software running on the processor (col. 3, lines 27-28; col. 4, line 49). As disclosed by Pai, processor 2 is not allowed to read the data in display buffer 40 during the GDP. Thus, this characterization of the isolated attribute clearly contradicts with the teaching of Pai.

Thus, for at least these reasons, Applicant respectfully submits that claim 15 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 15.

16. Regarding Claim 16

Claim 16 depends from claim 13 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 13, Pai in view of PC does not teach or suggest each of the elements of claim 16.

Moreover, claim 16 further recites "loading data from the isolated output area into a bit plane on a graphics card; and denying all external access to the bit plane." Pai in view of PC at least does not teach or suggest "loading data from the isolated output area into a bit plane on a graphics card." The Examiner characterizes display buffer 40 as the bit plane on the graphics card. However, nothing in cited references suggest that display buffer 40 is a bit plane. The Examiner has engaged in impermissible hindsight reconstruction as there is no teaching or suggestion of a bit plane in any of the cited references.

Thus, for at least these reasons, Applicant respectfully submits that claim 16 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 16.

17. Regarding Claim 17

Claim 17 depends from claim 16 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 16, Pai in view of PC does not teach or suggest each of the elements of claim 17.

Moreover, claim 17 further recites "defining a first window for display of an image corresponding to the bit plane; and occluding all windows but the first window." The windows occluded are all windows other than the first window, which is the window into which the isolated output area data from the bit plane on the graphics card is loaded. Stated differently, all non-isolated mode windows are occluded responsive to entry into the isolated mode. Accordingly, the official notice of ATM machines, even if well taken, and even if it did render obvious, "to one of ordinary skill in the art [to] occlude the image prior to transitioning out of isolated execution mode, in order to preserve the security information being displayed," is inapposite here. It is not the occlusion of information transitioning out of isolated execution mode that is being claimed. Rather, in claim 17, it is the occlusion of other windows upon the entrance into isolated execution mode that is claimed. The Examiner has persistently ignored this distinction notwithstanding that it has been raised repeatedly by Applicant.

Thus, for at least these reasons, Applicant respectfully submits that claim 17 is not obvious over Pai in view of PC. Thus, the Board should overturn the rejection of claim 17.

18. Regarding Claim 18

Claim 18 depends from claim 13 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 13, the cited references do not teach or suggest each of the elements of claim 18.

Moreover, claim 18 further recites "retrieving data from the isolated output area; displaying an image corresponding to the data; and occluding the image prior to a platform transitioning out of isolated execution mode." There is no motivation to combine the official notice of ATM machines with the cited references. The genetic code system of Pai and an ATM machine have divergent functions. Without viewing the

claim, a skilled person in the art would not be motivated to apply the operation of an ATM machine to the system of Pai. Thus, the Examiner has engaged in impermissible hindsight reconstruction in proposing the combination.

Thus, for at least these reasons, Applicant respectfully submits that claim 18 is not obvious over the cited references. Thus, the Board should overturn the rejection of claim 18.

19. Regarding Claim 19

In regard to independent claim 19, Applicant submits that the cited references at least fails to disclose or suggest the limitations of "a DMA controller", "the first interface coupled to the DMA controller to forward requests to a MCH" and "a second interface coupled to the DMA controller to supply output data to an output device."

As mentioned above in regard to claims 3 and 4, the cited references do not teach or suggest the DMA controller or the MCH. Moreover, there is nothing in the art that even remotely suggests a DMA controller that issues requests to a MCH and to supply output data to an output device.

The Examiner takes official notice that the second interface is well known in the art and is obvious to a skilled person because it allows the system to have more than one output. However, there is nothing in the art that suggests the interface be coupled to a DMA controller.

Thus, for at least these reasons, Applicant respectfully submits that claim 19 is not obvious over the cited references. Thus, the Board should overturn the rejection of claim 19.

20. Regarding Claim 20

Claim 20 depends from claim 19 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 19, the cited references do not teach or suggest each of the elements of claim 20.

Moreover, claim 20 further recites that "the first interface is a secure accelerated graphics port (AGP) and the output device is a display." As mentioned above in regard

to claim 9, none of the cited references disclose or suggest a secure accelerated graphics port. Thus, for at least these reasons, Applicant respectfully submits that claim 19 is not obvious over the cited references. Thus, the Board should overturn the rejection of claim 19.

21. Regarding Claim 21

Claim 21 depends from claim 19 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 19, the cited references do not teach or suggest each of the elements of claim 21.

Moreover, claim 21 further recites that "the DMA controller attaches an isolated attribute to any isolated output area access request." Not only do the cited references fail to mention a DMA controller, but they also fail to mention or suggest any device that "attaches an isolated attribute to any isolated output area access request" as claimed. The action of "attaching an isolated attribute" is completely missing in the cited references. Moreover, as mentioned above in regard to claim 15, the concept of isolated attribute is totally absent in the cited references. Thus, for at least these reasons, Applicant respectfully submits that claim 21 is not obvious over the cited references. Thus, the Board should overturn the rejection of claim 21.

22. Regarding Claim 22

Claim 22 depends from claim 19 and incorporates the limitations thereof. For at least the reasons mentioned above in regard to claim 19, the cited references do not teach or suggest each of the elements of claim 22.

Thus, Applicant respectfully submits that claim 22 is not obvious over the cited references. Accordingly, the Board should overturn the rejection of claim 22.

Based on the foregoing, the Board should **overturn** the rejection of all pending claims and hold that all of the claims currently pending in the application under review are allowable.

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Respectfully submitted,
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Amber D. Saunders 2/10/2006

Amber D. Saunders Date

VIII. CLAIMS APPENDIX

The claims involved in this appeal are presented below.

1. (Original) A platform comprising:

a processor executing in one of a normal execution mode and an isolated execution mode;

a system memory including an isolated area, an isolated output area, and a non-isolated area; and

an output device.

2. (Original) The platform of claim 1 wherein the output device is a graphics card.

3. (Original) The platform of claim 2 further comprising:

a memory control hub (MCH) coupled between the system memory, and the processor and the graphics card, the memory control hub to permit the graphics card to access the isolated output area only when the graphics card is in isolated access mode.

4. (Original) The platform of claim 3 wherein the graphics card comprises:

a direct memory access (DMA) controller and wherein local storage of the data from the isolated output area is not permitted.

5. (Original) The platform of claim 3 wherein only the graphics card is permitted to read the isolated output area.

6. (Original) The platform of claim 1 further comprising:

an operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in isolated execution mode.

7. (Original) The platform of claim 3 further comprising:

a link between the graphics card and the MCH having an isolated transaction type.

8. (Original) The platform of claim 3 wherein the MCH only permits the O/S nub to write to the isolated output area.

9. (Original) The platform of claim 7 wherein the link is a secure accelerated graphics port bus.

10. (Original) The platform of claim 2 wherein the graphics card comprises:

an isolated bit plane; and

a non-isolated bit plane.

11. (Original) The platform of claim 10 wherein the graphics card denies all external access to the isolated bit plane.

12. (Original) A method comprising:

establishing an isolated execution environment having an isolated execution mode; and

preventing access to output data by any requester not operating in an isolated mode.

13. (Original) The method of claim 12 wherein establishing comprises:

segregating a system memory into an isolated output area and a non-isolated area.

14. (Original) The method of claim 13 further comprising:

issuing an isolated direct memory access (DMA) request for display data in the isolated output area from a graphics card; and

refreshing the display based on the display data.

15. (Original) The method of claim 13 wherein preventing comprises:

identifying if an isolated attribute is present in a request for access to the isolated output area; and

denying the request if no isolated attribute is present.

16. (Original) The method of claim 13 further comprising:

loading data from the isolated output area into a bit plane on a graphics card; and

denying all external access to the bit plane.

17. (Original) The method of claim 16 further comprising:

defining a first window for display of an image corresponding to the bit plane; and

occluding all windows but the first window.

18. (Original) The method of claim 13 further comprising:

retrieving data from the isolated output area;

displaying an image corresponding to the data; and

occluding the image prior to a platform transitioning out of isolated execution mode.

19. (Original) A platform comprising:

a processor executing in one of a normal execution mode and an isolated execution mode;

a direct memory access (DMA) controller to issue requests for access to an isolated output area;

a first interface coupled to the DMA controller to forward requests to a memory control hub (MCH); and

a second interface coupled to the DMA controller to supply output data to an output device.

20. (Original) The apparatus of claim 19 wherein the first interface is a secure accelerated graphics port (AGP) and the output device is a display.

21. (Original) The apparatus of claim 19 wherein the DMA controller attaches an isolated attribute to any isolated output area access request.

22. (Original) The apparatus of claim 19 wherein the second interface is an audio interface.

IX. EVIDENCE APPENDIX

No evidence is submitted with this appeal.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings exist.